PARALLEL I/O BOARD

DOCUMENTATION UPDATE

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THEORY of OPERATION

PARALLEL I/O BOARD OPERATION

The Parallel I/O Board is designed to interface any 8-bit parallel device to the ALTAIR 8800. The board can be jumpered for any one of 128 addresses and has full hardware interrupt capability. An 8-bit latch for both the input word and the output word act as buffers between the ALTAIR and the external device.

Card Select

The board is selected from the bus by address lines A1 through A7 and the inversion of these lines, $\overline{A1}$ through $\overline{A7}$. When these seven address bits appear at the inputs of IC C as all logic ones (all inputs high), pin 8 of IC C will go low and enable pins 8 & 11 of IC D.

Channel Select

The P I/O Board has both a control channel and a data channel, either of which is selected by the state of address line A0. If the incoming address is an even number (A0 is low), IC D pin 10 will go high and select the control channel.

Control Channel

The control channel is used to test the status of the external device and to operate the interrupt enable/disable circuitry.

The data latches (OUT port IC G & IN port IC H) each contain an internal flip-flop that can be set by their "STB" input. The "STB" inputs may be pulsed high by the "handshake" lines to the external devices, "SBO" for the output device and "SBI" for the input device. These two signals are for the purpose of informing the CPU that the external device has sent or is ready to recieve data. When the "STB" input to these latches is pulsed high, the "$\overline{INT}$" output goes low signifing a ready condition for the particular device.

The "$\overline{INT}$" signals from both latches, G & H, are also buffered and sent to the external devices for additional "handshake" capability on lines "BO" and "BIN".

The control channel line is gated together with the "SINP" line at IC N, pins 9 & 10. When an "IN" instruction is followed by the even address of the board pin 8 of IC N goes low and partially enables IC O at pins 2 & 5, and enables two of the gates of IC L.

This places the status information onto the two status bit lines, DIO and DI1. If DIO is high, the output device is ready to recieve new data from the computer. If DI1 is high, the input device has sent data and the computer can now access it.

When an "OUT" instruction is followed by the even address of the board, the four gates of IC E in the interrupt control circuitry become partially enabled.

Data bits DO0 and DO1 are inverted then split and one signal inverted again. These four signals are fed into the remaining inputs of IC E. The outputs of IC E are fed through R-S flip-flops and some NOR gates to the vectored interrupt jumper lines.

The state of data bits DO0 and DO1 is used to determine which of the interrupt lines will be enabled. If DO0 is high, the output device interrupt is enabled. If DO1 is high, the input device interrupt is enabled. If the "BOTH" jumper is used, then either signal being high will cause an interrupt.

Data Channel

If the incoming address for the board is the odd address (A0 is high), IC D pin 13 will go high selecting the data channel.

When the signal on IC D pin 13 goes high IC H is partially enabled, along with one gate of IC N at pin 2. When the "SINP" signal goes high the IC H latch becomes completely enabled, and IC N pin 3 is enabled. The signal at IC N pin 3 enables the data buffers from latch H, placing the data on the bus lines DI0 through DI7.

For an output instruction, the odd address again partially enables IC G through IC D pin 13.

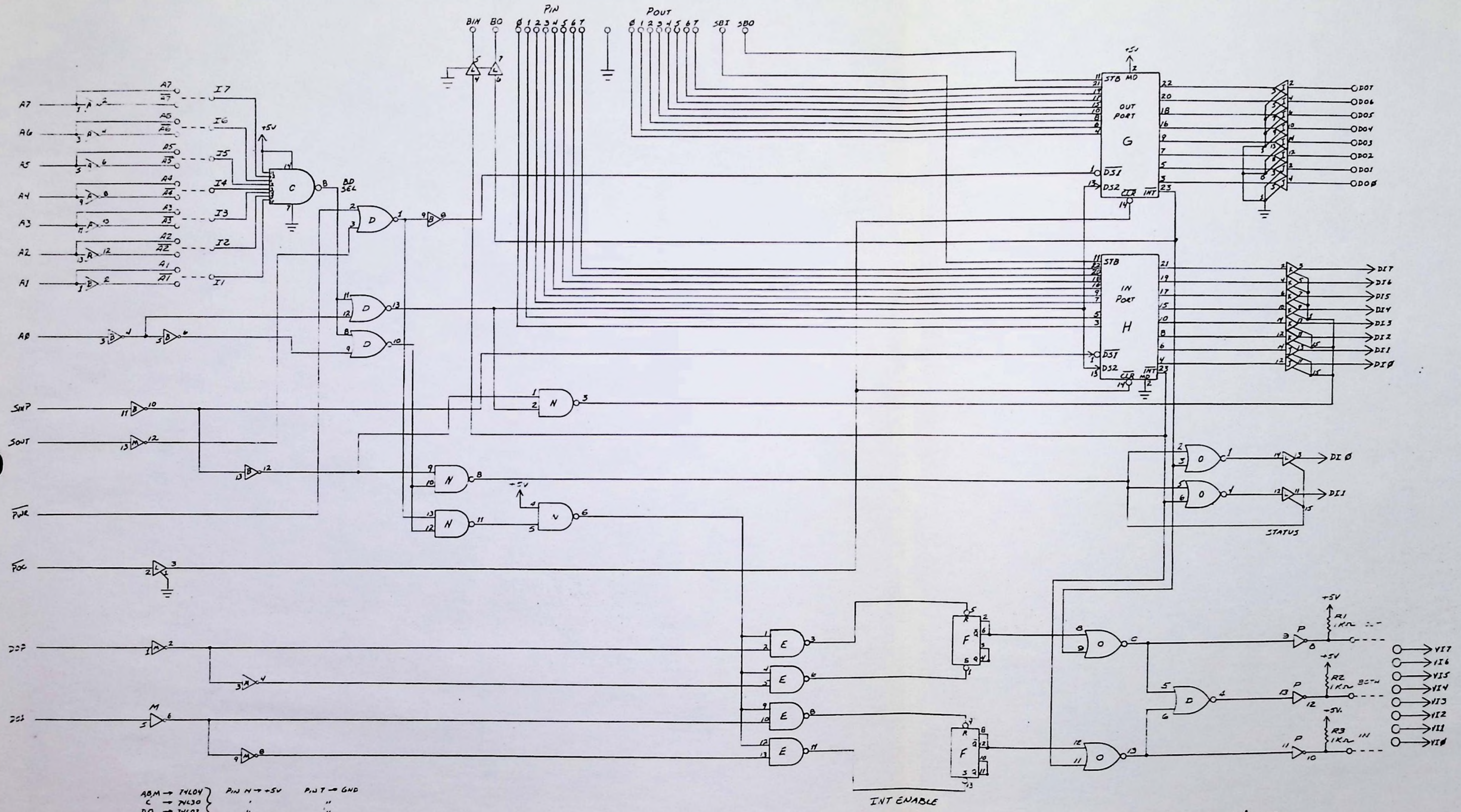
When the "OUT" instruction is executed the "SOUT" signal goes high, followed by "$\overline{\text{PWR}}$" going low. This enables IC D pin 1, which in turn completely enables IC G. This causes the data present on the bus to be latched into IC G.

Interrupt

The pads "OUT", "IN" and "BOTH" may be jumpered to the pads VI0 through VI7 to provide hardware interrupt capability for the board. The first three pads represent the OUTput device, the INput device and BOTH devices. The pads VI0 through VI7 are the interrupt lines which connect to the Vectored Interrupt Board (88-VI), and the 0 to 7 portion corresponds to the 8 priority levels with 0 the lowest and 7 the highest priority.

The input device and the output device may each be assigned a different priority, or both devices may be assigned a single priority. If the 88-VI board is not in the system, one of the three pads, "OUT", "IN" or "BOTH", on one of the I/O boards may be jumpered to the CPU input interrupt line. (see assembly procedure)

The last method above will allow one level of interrupt to the CPU. When the interrupt occurs, the processor will immediately jump to the location 70 (octal) and begin execution. Place the interrupt service routine in locations 70 through 77 (octal).



A,B,M → 74LS04	PIN N → +5V	PIN T → GND
C → 74LS30	"	"
D,O → 74LS02	"	"
E,F,N → 74LS00	"	"
G,H → 8212	PIN 24 → +5V	PIN 12 → GND
I,J,K,L → 8T97	PIN 16 → +5V	PIN 8 → GND

PARALLEL I/O BD